REMARKS

Applicant respectfully requests reconsideration of this application as amended.

By this Amendment, independent Claim 20 has been amended to include means for checking the integrity information and at least a databus, wherein the transmitting of information through the databus is secured and that it comprises . . . reading, by the processing means, of said information transmitted from the storage means to the processing means for processing via a databus and processing said information and verifying, by the processing means or by the means for checking the integrity of information, during the processing of the specific condition as satisfied.

Independent Claim 29 has been amended to include means for checking the integrity of information, the processing means selecting information extracted from the storage means in order to process it, the means for disabling being activated when the means for verification or means for checking the integrity of information have detected that the specific condition is not satisfied.

Support for the above amendments can at least be found on pages 4, 5, and 7.

In contrast, Holtey includes a memory chip having an access control unit and, as specified on column 3, line 28 of Holtey, the validation operation is carried out with a host computer. Therefore, the access control unit in the chip of Holtey does not process information contained in the memory since it only has to control the access to information. Thus, the chip described in Holtey can only be a slave module. Moreover, in Holtey, with reference to Fig. 3, the result of the authentication procedure induces the state of the access control memory (43) which enables the output buffer (52). Holtey specifies on column 8, line 12 that the output of the access control (43) is applied as an enabling input to output buffer (52) during each memory read cycle. As a consequence,

the transfer of information on the databus is not secured when the output buffer is enabled.

In Hazard, and in particular page 1, line 14, Hazard states that the term monolithic security module covers any electronic circuit constitute by a silicone chip. Applicant respectfully submits it is obvious that monolithic chips can be master or slave working modules. Moreover, in Hazard page 2, line 21, it is stated that an object of the invention is to detect alterations in the transmission between a memory and a microprocessor. A first embodiment is described on page 4, line 30 where a hacker sends radiation through the bus. It is specified on page 5 lines 4-5 that by emitting the radiation, the microprocessor will read bytes at "00". It is then stated on page 5, lines 16-17 of Hazard that a solution consists of interrupting a normal operation of the microprocessor during the reading of an instruction whose code is "00" or "FF". Consequently, the transfer of data on databus is secured in relation to radiation of hackers on the databus.

In Holley, with reference to column 3, lines 24-26, it is specified that bits of a key value are compared against the bit contents of lock bit positions on the memory block. It is described with reference to Figs. 2 and 4 that keys are stored in the access control processor and that lock bits 54a are stored in the memory. A lock bit and key bits are compared in a bit logic comparator so that comparator 30-1 receives key bits from the access control processor 10 and from a memory block 54, the result being sent to the access control memory 43, which controls the output buffer 52 of the memory. In Hazard, with reference to page 6, lines 19-23 an integrity check element is implemented from one end of the bus to the other with the wiring diagram and its bus integrity controller being illustrated in Fig. 4. It is specified on page 7, lines 4-6 that the means for checking the integrity comprises parity generators 7, 8, and 11 and it is also specified that

the parity generator 8 calculates the parity of the data selected in the ROM. The information is read in the memory by the processing means and, with reference to Fig. 4 of Hazard, the calculated piece of integrity data is compared by means for checking the integrity of information. Moreover, the means for checking the integrity of information has a connection to the NMI input of the processor.

As a result, when the processing means are reading information from the storage means, the means for checking the integrity of information operates on the information received by the processing means. In contrast, in Holtey, the information is sent by an access control processor 10 to a comparator 30-1. In Holtey, the information is read in a memory block 54 by a processor which is external to the chip.

Moreover, in Hazard the means for checking the integrity of information acts on the processor, which processes the information. In Holtey, the component makes a comparison acts on the output buffer(52) of the memory.

The independent claims are thus clearly patentably distinguishable from the cited references.

With regard to Claim 26, Applicant respectfully submits that Holtey at no point mentions the fact that it is a microprogrammed instruction. With reference to Claim 28, it is specified in Holtey that a second type of instruction is executed to compare a key bit to a corresponding lock bit. It is also stated that a third type of instruction sets the block access control memory bit only when the results are correct. Holtey at no point teaches or suggests disabling the component when fraud is detected.

Regarding Claim 33, Applicant respectfully submits that the disabling means is neither taught nor suggested by any of the cited references. Moreover, with reference to

Claim 34, it is respectfully submitted that none of the references of record teach or suggest the claimed parity generator.

With all rejections having been overcome, and the claims being clearly patentably distinguishable from the references of record, Applicant respectfully submits that the application is in condition for allowance. A prompt Notice of Allowance is respectfully solicited.

Should the Examiner believe that any further action is necessary to place this application in better form for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T2146-906833) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By:
Edward J. Kondracki
Reg. No. 20,604

Jason H. Vick
Reg. No. 45,285

JHV:jab

Miles & Stockbridge P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
(703) 903-9000
August 15, 2005
#9277499

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on August 15, 2005.

Jason H. Vick